REMARKS

Favorable reconsideration, in light of the present amendment and the following discussion, is respectfully requested.

After entry of the foregoing amendment, Claims 30 and 31 are pending in the present application. Claims 30 and 31 are amended without introduction of new matter.[1]

In the outstanding Office Action, Claims 30 and 31 were rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,366,488 to Zambrano et al. (hereinafter "Zambrano"); Claims 30 and 31 were rejected under 35 U.S.C. 102(b) as anticipated by *A Sub-40-NS Chain FRAM Architecture with 7-ns Cell-Plate-Line Drive* to Takashima et al. (hereinafter "Takashima"); and Claim 30 was rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,759,251 to Ozaki.

Turning now to the rejections of Claims 30 and 31 under 35 U.S.C. 102, summarized above, those rejections are respectfully traversed.

Though Claims 30 and 31 are different in scope, each of those claims recites "covering the second upper electrode with insulating layer, such that the second upper electrode is insulated from the first and second impurity-diffused regions by the insulating layer and the ferroelectric layer."

Applicants' "Discussion of the Background" addresses a micro loading effect, in which the distance between features affects the rate at which they are etched; and, consequently, affects their size, as well.[2] As shown in Figure 34, for example, the capacitor of word line WL1 is an outermost capacitor, as compared to the capacitors of word lines WL2 to WL7. An upper electrode forming the capacitor of word line WL1 is an outermost upper electrode, as compared to the upper electrodes forming the capacitors of word lines WL2 to W7. Thus, during fabrication, the upper electrode forming the capacitor of word line

[1] For support, see Applicants' discussion of Figure 1, *infra*.
[2] Specification, page 3, lines 10-15; page 7, line 32 – page 8, line 4.

WL1 may etch more quickly than the upper electrodes forming the capacitors of word lines WL1 to WL7. In this example, the upper electrode forming the capacitor of word line WL1 is an outermost upper electrode because of its placement next to a block selecting transistor 6.

Figure 1 illustrates a non-limiting example of the second upper electrode of amended Claims 30 and 31. As shown, a dummy upper electrode 25 is arranged over a block selecting transistor 6; and adjacent to a first upper electrode 20. The dummy upper electrode 25 is insulated from second and third impurity regions 112, 114 by an insulating layer 60 and a first ferroelectric layer 19. Unlike the dummy upper electrode 25, the first upper electrode 20 forms a functional capacitor connected to the second and third impurity regions 112, 114.[3] The placement of the dummy upper electrode 25 reduces the micro loading effect on the first upper electrode 20, which in turn provides greater control of the etch rate and size of the first upper electrode 20.

The outstanding Office Action does not address the second upper electrode of amended Claims 30 and 31. Applicants submit that the applied references do not teach the above-noted feature of "covering the second upper electrode with insulating layer, such that the second upper electrode is insulated from the first and second impurity-diffused regions by the insulating layer and the ferroelectric layer."

Accordingly, Applicants respectfully request that the rejections of Claims 30 and 31 under 35 U.S.C. 102, summarized above, be withdrawn.

[3] Specification, page 12, lines 1-11.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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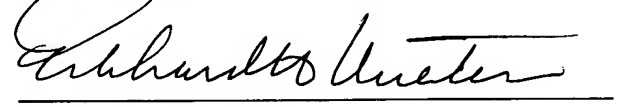

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